device (found also in the applicant's letter dated April 15, 2005, page 15, paragraph 4 till page 16 paragraph 2), must be placed in the section "Detailed Description of the Preferred Embodiments" after the paragraph [0100], more precisely in the freeing space between the paragraph [0100] and the old paragraph [0109]. A copy of this amendment to the specification is the follow:

"A second embodiment of the proposed VLSI device for implementing in hardware any multiple-output combinational target circuit defined by a group of logical sum-of-product equations, considers every single sum-of-products logical equation as an independent equation. Each independent equation needs a maximum of q modified cells C(k), where a modified cell C(k) is used for determining the logical value of a product term p(k) of an independent equation. If the same product term is a component of several independent sum-of-product equations, this product term must be implemented several times in hardware, using a modified cell C(k) for each equation where the product term is there.

Let's assume that for this second embodiment, a multiple output target combinational circuit has the following equation that gives one of the outputs (the same equation as used for Z in (1)):

$$Z = a.b + \bar{a}.\bar{b}.\bar{c} + \bar{c}.\bar{d} \qquad (8)$$

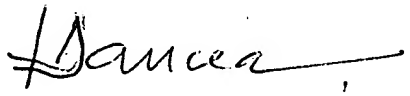
Fig. 10 demonstrates how the mask words and the product words are applied to the associated inputs (a = 1, b = 1, c = 0, d = 1) to provide the output of the considered independent equation (8). Fig. 11 shows partially the second embodiment of the proposed VLSI device, the structure 41 implementing only the independent equation (8). Each independent equation uses q modified cell C(k) 42, as shows in Fig. 12. The modified cell 42 has only the mask word register 32 and the product word register 33 connected to the associated combinational part, formed by AND gates 35, EQUIVALENCE (XNOR) gates 36, and AND gate 37. In Fig. 11 one and only one final OR gate 39 is used to determine the logical value of the single output of the independent equation. This second embodiment

of the proposed VLSI device can be equally used to implement the sum-of-product logical equations that describe the combinational parts of sequential target circuits".

(2) Applicant's Figure A, B, C and attached explications were introduced only to support the arguments for overcoming examiner's rejection of claims, and particularly of the old claim 1. As correctly assumed by the examiner, the applicant does not consider Figures A, B and C as part of the drawings in this application. So, please do not consider these figures among the drawings of the application.

(3) The applicant's amendment to claims 8, 9, and 13-15 included improper dependent forms and consequently these claims have been rephrased (enclosed herewith is a clean copy of all claims, the reformulated claims marked with "Currently amended" and the non-modified claims marked with "Previously presented", as its were formulated in the applicant's correspondence dated April 15, 2005). The applicant hopes that the new dependent claims are correct.
Thank you for your assistance.

Yours truly, applicant



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